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10/562,303	12/22/2005	Axel Andersch	2003P08945WOUS	3763

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EXAMINER	
THANGAVELU, KANDASAMY	
ART UNIT	PAPER NUMBER
2123	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/562,303	ANDERSCH ET AL.	
	Examiner	Art Unit	
	KANDASAMY THANGAVELU	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 December 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *12-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *12-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *12/22/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 12-22 of the application have been examined.

Foreign Priority

2. Acknowledgment is made of applicant's claim for foreign priority based on an application 10329147.4 filed in Germany on 27 June 2003 and the PCT EP/2004/004991 filed in Germany on 10 May 2004. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Information Disclosure Statement

3. Acknowledgment is made of the information disclosure statements filed on December 22, 2005 together with a list of patents and copies of papers. The patents and papers have been considered.

Drawings

4. The drawings submitted on December 22, 2005 are accepted.

Claim Objections

5. The following is a quotation of 37 C.F.R § 1.75 (d)(1):

> The claim or claims must conform to the invention as set forth in the remainder of the specification and terms and phrases in the claims must find clear support or antecedent basis in the description so that the meaning of the terms in the claims may be ascertainable by reference to the description.

6. Claim 19 is objected to because of the following informalities:

In Claim 19, Line 2, "at least a part of the signals in comprises a third partial area" appears to be incorrect and it appears that it should be "at least a part of the signals in a third partial area".

Appropriate correction is required.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.

8. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

9. Claims 12, 14, 16, 17, 19 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Swaboda et al.** (U.S. Patent Application 2003/0200425), in view of **Agarwala et al.** (U.S. Patent 6,948,155).

9.1 **Swaboda et al.** teaches efficient model order reduction via multi-point moment matching. Specifically as per claim 12, **Swaboda et al.** teaches a system for combining and representing signals of a hardware simulation device and elements of a listing of a software program (Fig. 44; Fig. 46; Fig. 51; Fig. 52; Page 1, Para 0024; Page 2, Para 0030, L1-8 and L15-19), comprising:

a graphical display (Fig. 45: User interface, window driven; Page 5, Para 0111; Page 5, Para 0112, L5-9);

a software program (Page 3, Para 0083; Page 5, Para 0111);

a listing of the soft-ware program having listing elements (Page 3, Para 0083; Page 5, Para 0111); and

a hardware simulation device configured to simulate a behavior of a circuit (Page 3, Para 0082, L4-6; Fig. 44, Items 1101 and 1131; Fig. 46;, Item 1101 and Item 1043; Page 7, Para 0134) having a processor (Fig. 46, Item 1043), a program memory including a program code of

the software program (Page 4, Para 0094, L1-4) and application-specific hardware components (Page 4, Para 0091, L5-7; Para 0096; Page 7, Para 0134); and

create signals during a simulated execution of the program code included in the program memory (Page 4, Para 0091, L1-5; Page 4, Para 0093; Para 0095, L1-3), the program code corresponding to the listing elements (Page 3, Para 0083; Page 5, Para 0111), the signals representing a result of the hardware simulation (Page 6, Para 0116, L1-5; Para 0119, L1-4; Para 0122, L1-5; Para 0125 and Para 0126), wherein the system is programmed and configured to:

display the listing elements in a first partial area of the graphical display (Page 5, Para 01017, Memory and status registers; Para 0110, L4-7; Para 0111, L1-8; Para 0112, L5-6); and

display the signals in a second partial area of the graphical display (Page 5, Para 0107, status of target chip; Page 5, Para 0111, L1-4; Para 0112, L5-9; Page 6, Para 0116, L1-5; Para 0119, L1-4; Para 0122, L1-5; Para 0125 and Para 0126).

Swaboda et al. does not expressly teach a hardware simulation device configured to interrelate the listing elements with the signals. **Agarwala et al.** teaches a hardware simulation device configured to interrelate the listing elements with the signals (Fig. 2; CL3, L60 to CL4, L2; CL4, L8-15). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the system of **Swaboda et al.** with the system of **Agarwala et al.** that included a hardware simulation device configured to interrelate the listing elements with the signals, because that would allow provide means to record and display chip activity of interest during debugging of the application program with the correlation of source code with chip activity (CL4, L8-15).

In addition:

Hellastrand et al. (U.S. Patent Application 2002/0032559) teaches hardware simulation and simulating execution of user program together and showing the results from both simultaneously (Fig. 1; Abstract; Page, Para 0002, L3-6 and L12-14; Para 0005, L1-5; Page 8, Para 0089, L1-6).

Rostoker et al. (U.S. Patent 6,470,482) teaches displaying listing of user program and HDL code of the circuitry on different windows of the user interface system of a simulation system (Fig. 13, 14 and 15). The schematics and other information of the hardware are also shown in additional windows.

Per claim 14: **Swaboda et al.** teaches that the graphical display comprises a third partial area for representing at least a part of the signals (Page 4 and 5, Para 0100; Page 5, Para 0111; Para 0112, L5-9).

Per claim 16: **Swaboda et al.** teaches an adapting unit for adapting the system to different processor types (Fig. 46, Items 1141 and 1043).

9.2 As per Claims 17 and 19, these are rejected based on the same reasoning as Claims 12 and 14, supra. Claims 17 and 19 are method claims reciting the same limitations as Claim 12 and 14, as taught throughout by **Swaboda et al.** and **Agarwala et al.**

9.3 As per claim 22, **Swaboda et al.** teaches an error locating tool for combining and representing signals of a hardware simulation device and elements of a listing of a software program (Fig. 44; Fig. 46; Fig. 51; Fig. 52; Page 1, Para 0024; Page 2, Para 0030, L1-8 and L15-19),

the hardware simulation device configured to simulate a behavior of a circuit (Page 3, Para 0082, L4-6; Fig. 44, Items 1101 and 1131; Fig. 46;, Item 1101 and Item 1043; Page 7, Para 0134) with a processor (Fig. 46, Item 1043), with a program memory having a program code of the software program (Page 4, Para 0094, L1-4) and with application-specific hardware components (Page 4, Para 0091, L5-7; Para 0096; Page 7, Para 0134); and

the hardware simulation device further configured to create signals as a result of a simulation (Page 4, Para 0091, L1-5; Page 4, Para 0093; Para 0095, L1-3; Page 6, Para 0116, L1-5; Para 0119, L1-4; Para 0122, L1-5; Para 0125 and Para 0126), the program code corresponding to the listing elements (Page 3, Para 0083; Page 5, Para 0111), the error locating tool comprising:

a graphical display for displaying the elements in a first partial area of the graphical display (Page 5, Para 01017, Memory and status registers; Para 0110, L4-7; Para 0111, L1-8; Para 0112, L5-6); and

a graphical display for displaying the signals interrelated with the elements in a second partial area of the graphical display (Page 5, Para 0107, status of target chip; Page 5, Para 0111, L1-4; Para 0112, L5-9; Page 6, Para 0116, L1-5; Para 0119, L1-4; Para 0122, L1-5; Para 0125 and Para 0126).

Swaboda et al. does not expressly teach the error locating tool comprising an analysis unit for interrelating the elements of the listing with the signals created during a simulated execution of the program code. **Agarwala et al.** teaches the error locating tool comprising an analysis unit for interrelating the elements of the listing with the signals created during a simulated execution of the program code (Fig. 2; CL3, L60 to CL4, L2; CL4, L8-15).

10. Claims 13 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Swaboda et al.** (U.S. Patent Application 2003/0200425), in view of **Agarwala et al.** (U.S. Patent 6,948,155), and further in view of **Mc Connell et al.** (U.S. Patent Application 2001/0049593) and **Choi et al.** (U.S. Patent Application 2003/0004699).

10.1 As per claim 13, **Swaboda et al.** and **Agarwala et al.** teach the system of claim 12. **Swaboda et al.** and **Agarwala et al.** do not expressly teach a marking unit for marking at least one of the listing elements in the first partial area. **Mc Connell et al.** teaches a marking unit for marking at least one of the listing elements in the first partial area (Page 6, Para 0074, L1-6; Para 0081; Para 0082, L1-4). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the system of **Swaboda et al.** and **Agarwala et al.** with the system of **Mc Connell et al.** that included a marking unit for marking at least one of the listing elements in the first partial area, because that would allow indicating to the user the code that was currently being executed (Para 0082, L1-4).

Agarwala et al. teaches signals interrelated with the at least one listing element (Fig. 2; CL3, L60 to CL4, L2; CL4, L8-15). **Swaboda et al., Agarwala et al.** and **Mc Connell et al.** do

not expressly teach a marking unit for marking such signals interrelated with the at least one marked listing element in the second partial area. **Choi et al.** teaches a marking unit for marking such signals in the second partial area (Fig. 8; Page 4, Para 0054; Page 5, Para 0055). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to combine the system of **Swaboda et al., Agarwala et al.** and **Mc Connell et al.** with the system of **Choi et al.** that included a marking unit for marking such signals in the second partial area, because that would allow identifying a significant point in time in simulation and highlight across the signal or waveform and correlate it to the source code (Page 5, Para 0055).

10.2 As per Claim 18, it is rejected based on the same reasoning as Claims 13, supra. Claim 18 is a method claim reciting the same limitations as Claim 13, as taught throughout by **Swaboda et al., Agarwala et al., Mc Connell et al.** and **Choi et al.**

11. Claims 15, 20 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Swaboda et al.** (U.S. Patent Application 2003/0200425), in view of **Agarwala et al.** (U.S. Patent 6,948,155), and further in view of **Hellestrand et al.** (U.S. Patent Application 2002/0032559).

11.1 As per claim 15, **Swaboda et al.** and **Agarwala et al.** teach the system of claim 12. **Swaboda et al.** and **Agarwala et al.** do not expressly teach that the circuit is described in a hardware description language. **Hellestrand et al.** teaches that the circuit is described in a hardware description language (Abstract; Fig. 1, Item 103; Fig. 10; Fig. 11; Page 1, Para 0006,

L1-7; Page 2, Para 0012, L1-5; Page 3, Para 0023, L1-3; Page 6, Para 0070, L1-6). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the system of **Swaboda et al.** and **Agarwala et al.** with the system of **Hellestrand et al.** that included the circuit being described in a hardware description language, because the hardware processor is usually specified in a hardware description language (Page 1, Para 0006, L1-4); and the digital circuitry is usually specified in a hardware description language (Page 3, Para 0023, L1-3).

11.2 As per Claim 20, it is rejected based on the same reasoning as Claims 15, supra. Claim 20 is a method claim reciting the same limitations as Claim 15, as taught throughout by **Swaboda et al., Agarwala et al.** and **Hellestrand et al.**

11.3 As per claim 21, **Swaboda et al.** and **Agarwala et al.** teach the method of claim 17. **Swaboda et al.** and **Agarwala et al.** do not expressly teach adapting such hardware description language corresponding to the processor to represent a different Processor type. **Hellestrand et al.** teaches adapting such hardware description language corresponding to the processor to represent a different Processor type (Abstract; Fig. 1, Item 103; Fig. 10; Fig. 11; Page 1, Para 0006, L1-7; Page 2, Para 0012, L1-5; Page 3, Para 0023, L1-3; Page 6, Para 0070, L1-6; Page 1, Para 0004).

Conclusion

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dr. Kandasamy Thangavelu whose telephone number is 571-272-3717. The examiner can normally be reached on Monday through Friday from 8:00 AM to 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Paul Rodriguez, can be reached on 571-272-3753. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to TC 2100 Group receptionist: 571-272-2100.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only.

For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Kandasamy Thangavelu/
Art Unit 2123
September 10, 2008